GENERATION OF HIGH-SPEED PSEUDO-RANDOM SEQUENCES USING MULTIPLEX-TECHNIQUES

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ABSTRACT

We report on the design and performance of high-speed pseudo-random sequence generators for NRZ-signals. The hardware is based on multiplexer circuits that multiply the data rate of a 5 Gbit/s pseudo-random sequence to respectively 10 Gbit/s and 20 Gbit/s. We used multiplex-techniques based on the „cycle-and-add property" of pseudo-random sequences. Using both microstrip and coplanar waveguide technology, the circuitry incorporates special high-speed silicon chips. The experimental results demonstrate the feasibility of our approach.

INTRODUCTION

The present work arose from a requirement of high-speed pattern generation for the development of modern optical data transmission systems. Using special multiplex-techniques [1] and considering the "cycle-and-add-property" [2], fast pseudo-random sequences can be obtained by multiplying the data rates of sequences which are derived from low-speed pulse pattern generators. For a reasonable hardware implementation it is important that long delay times are avoided by the use of EXOR operations in order to maintain the maximum word length at the output of the multiplying stages.

First, the multiplex-technique is described and applied to a standardized sequence [3] using a length of $L = 2^{23}-1$ bits. Based on that principle, a circuit is described which generates a 10 Gbit/s pseudo-random sequence. In a next step, a 20 Gbit/s sequence is generated utilizing coplanar waveguide technology. Finally, a 20 Gbit/s pseudo-random sequence can be achieved.

TH 2A

OPERATIONAL PRINCIPLE

According to Eier and Malleck [1], generation of pseudo-random sequences can be described by the quotient of a decoupling polynomial and a feedback polynomial. This quotient can also be described by an infinite series as

$$\frac{H(D)}{A(D)} = m_1 D^0 \oplus m_1 D^1 \oplus \ldots = \sum_{r=0}^{\infty} m_r D^r . \qquad (1)$$

Separating this series in even and odd clock cycles

$$\frac{H(D)}{A(D)} = \left(\sum_{r'=0}^{\infty} m_{2r'} D^{2r'} \right) + D \left(\sum_{r'=0}^{\infty} m_{2r'+1} D^{2r'} \right), \qquad (2)$$

we obtain two series at a lower data rate that must be identical with the original one [4] (not considering a phase shift). On the other hand, inverting this procedure by combining two slower ones, the generation of a fast sequence is described by

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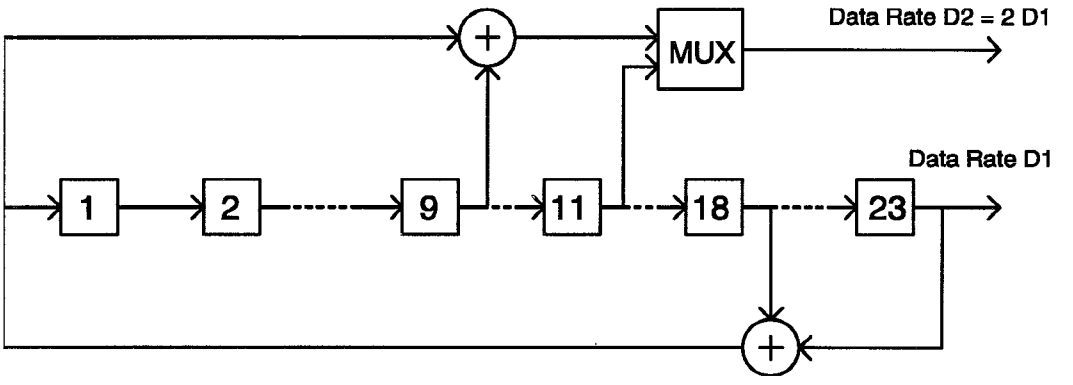

Fig. 1: *Operational principle.*

$$\frac{H(D)}{A(D)} = \frac{G(D^2)}{A(D^2)} + D \cdot \frac{U(D^2)}{A(D^2)} \quad . \tag{3}$$

For these kind of polynomials we have [2]

$$(P(D))^2 = P(D^2) \ , \tag{4}$$

yielding the slower sequence

$$G(D) = (H(D) \cdot A(D))_{even} \tag{5}$$

$$D \cdot U(D) = (H(D) \cdot A(D))_{odd} \ . \tag{6}$$

Since we need not consider the phase of the generated sequence, we set

$$H(D) \equiv 1 \ . \tag{7}$$

Applied to the CCITT standard sequence given in [3], we obtain the block diagram shown in Fig. 1. Since we do not have access to the internal shift register stages, the different sequences are provided by delayed versions of the output sequence.

CIRCUIT PRINCIPLE

For the realization of the 20 Gbit/s pseudo-random multiplier, circuits were used, which were fabricated in a silicon bipolar laboratory technology [5]. The circuits are based on E^2CL-logic in differential operation. An excellent performance is achieved because all inputs and outputs are terminated with 50Ω on-chip resistors providing very good matching and reducing the time-jitter. Furthermore, the circuits work with only a single supply voltage of -5V consuming 280mW of power.

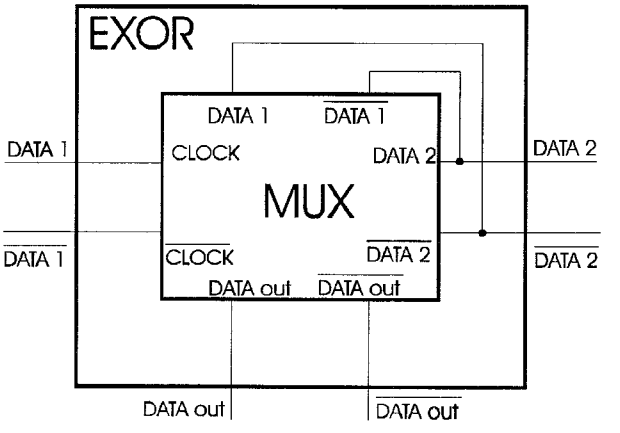

Fig. 2: *Realization of the EXOR-Gate using a multiplexer.*

The EXOR-gate was built using a multiplexer-chip, where the clock is used as the first input of the EXOR and the combination of data 2 and the inverted data 1 is used as the second input (Fig. 2).

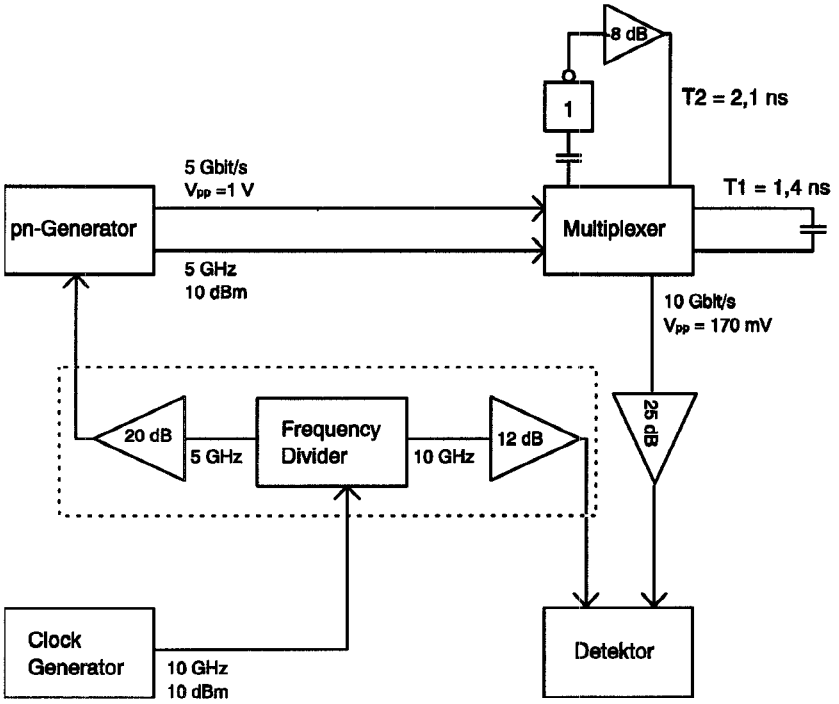

Fig. 3: *10 Gbit/s block diagram.*

EXPERIMENTAL RESULTS

A circuit providing a 10 Gbit/s pseudo-random sequence was realized in microstrip technology on a standard alumina substrate. The NRZ input signal is split into three paths 1, 2 and 3. The signal of path 1 is fed to an EXOR gate circuit whose second input is the NRZ input signal delayed by 9 bits. The output signal of the EXOR chip is one of the input signals of the multiplexer. The second multiplexer input signal is given by the NRZ input signal delayed by 11 bits. The delay times are provided by external coaxial lines. The chips, which here are operated single-endedly, are mounted into the substrate and are contacted by bond wires. To synchronize generator and detector, a frequency divider stage is used to provide appropriate clock signals. Fig. 3 shows the complete block diagram including frequency divider and delay lines. A further structure using two multiplexers generates a 20 Gbit/s sequence (Fig. 4).

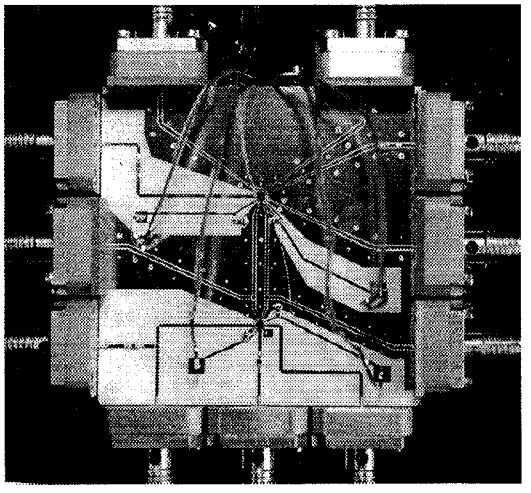

Fig. 4: *20 Gbit/s circuit.*

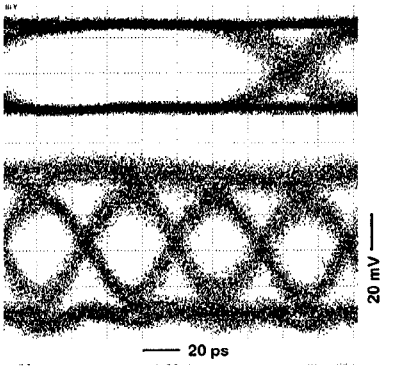

Fig. 5: *Eye diagram of a 5 Gbit/s input and a 20 Gbit/s output sequence.*

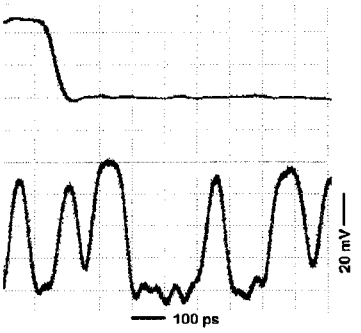

Fig. 6: *Portion of a 5 Gbit/s input and a 20 Gbit/s output sequence.*

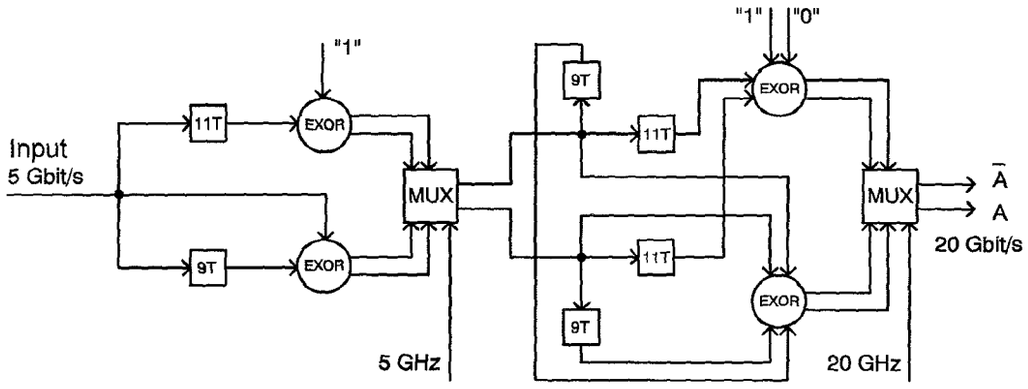

Fig. 7: *Block diagram to generate a 20 Gbit/s pseudo-random sequence.*

Due to the high data rate, the chips are operated differentially. The RF interconnection lines were fabricated in coplanar waveguide technology. To synchronize the single stages, all clock signals are provided by a frequency divider stage. Figs. 5 and 6 show respectively the eye diagram and portions of the 5 Gbit/s input and of the 20 Gbit/s output signal. Fig. 7 gives the block diagram of a circuit generating a 20 Gbit/s pseudo-random sequence. Additional EXOR-chips in both stages enable symmetrical operation of the multiplexers as well as differential operation of all important chips. Connections are made using coplanar waveguides that are tapered to contact both the chips and the plugs.

CONCLUSION

We succesfully used a multiplex-technique allowing to multiply the data rate of a 5 Gbit/s pseudo-random sequence to 10 Gbit/s. A 20 Gbit/s circuitry permits the derivation of a block diagram of a circuit which allows the generation of a 20 Gbit/s pseudo-random sequence using the same operational principle, operating all chips differentially and employing coplanar waveguide technology.

ACKNOWLEDGMENT

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